

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Addease COMMISSIONER POR PATENTS PO Box 1450 Alexandra, Virginia 22313-1450 www.wepto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
	PILING DATE			
10/632,089	08/01/2003	Olav Tirkkonen	59643-00238	3395
32294 7590 SQUIRE, SANDERS & DEMPSIEY LL.P. 8000 TOWERS CRESCENT DRIVE 14TH FLOOR VIENNA, VA 22182-6212			EXAMINER	
			NGUYEN, DUC M	
			ART UNIT	PAPER NUMBER
			2618	
			MAIL DATE	DELIVERY MODE
			07/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# UNITED STATES PATENT AND TRADEMARK OFFICE

# BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte OLAV TIRKKONEN and PIRJO PASANEN

Appeal 2008-2244 Application 10/632,089<sup>1</sup> Technology Center 2600

Decided: July 31, 2008

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and KARL D. EASTHOM, *Administrative Patent Judges*.

JEFFERY, Administrative Patent Judge.

 $<sup>^{\</sup>rm 1}$  This application claims benefit of Application 60/450,328, filed February 28, 2003.

#### DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-23. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

### STATEMENT OF THE CASE

Appellants invented a communication system for transferring data between a transmitter and a receiver over plural channels. The system includes circuitry for (1) determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and (2) selecting a bit loading sequence with a lowest error rate.<sup>2</sup> Claim 1 is illustrative:

1. A communication system for transferring data between a transmitter and a receiver over a plurality of channels, the communication system comprising:

modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences;

circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate; and

circuitry configured to select a bit loading sequence with a lowest error rate.

The Examiner relies on the following prior art references to show unpatentability:

Sadjadpour US 2001/0055332 A1 Dec. 27, 2001 Kim US 2003/0128769 A1 Jul. 10, 2003

<sup>&</sup>lt;sup>2</sup> See generally Spec. ¶¶ 0022-27.

Application 10/632,089

Appellants' admitted prior art from Paragraphs 0005 through 0020 and Figure 1 of the present application ("APA").

- Claims 1, 18, and 23 stand rejected under 35 U.S.C. § 102(a)<sup>3</sup> as being anticipated by Sadiadpour.
- Claims 2-13, 19, 20, and 22 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sadjadpour and APA.
- Claims 14-17 and 21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Sadjadpour, APA, and Kim.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

# The Anticipation Rejection

We first consider the Examiner's anticipation rejection of claims 1, 18, and 23 over Sadjadpour (Ans. 3-4). Regarding independent claim 1, Appellants argue that Sadjadpour fails to disclose circuitry configured to (1) determine a power allocation for at least one bit loading sequence based on minimizing an error rate, and (2) select a bit loading sequence with a lowest error rate, as claimed. According to Appellants, Sadjadpour merely selects a

\_

<sup>&</sup>lt;sup>3</sup> This reference actually qualifies as prior art under § 102(b) since it published more than one year before the effective filing date of the present application (Feb. 28, 2003). Nevertheless, we consider this error harmless as it does not affect our decision regarding the merits of the anticipation rejection.

specific constellation of symbols or bits creating symbols for each subfrequency bin dependent on minimizing power and cross talk. Additionally, Appellants argue, Sadjadpour's power allocation is based only on reducing cross talk, and not for at least one bit loading sequence based on minimizing the error rate, as claimed (App. Br. 7-10). Appellants make similar arguments with respect to independent claims 18 and 23 which recite commensurate limitations (App. Br. 10-16; Reply Br. 4).

The Examiner takes the position that since Sadjadpour's bit and power allocation algorithm involves selecting a function that minimizes the bit-error rate (BER), namely Function 62 in Figure 6, such an algorithm would also involve selecting the lowest BER (Ans. 8-11). Appellants, however, contend that the Examiner's reliance on Function 62 is flawed since this function jointly *minimizes* BER and *maximizes* the total data rate. As such, Appellants argue, function 62 does not absolutely minimize the BER since it must also maximize the total data rate (Reply Br. 3; emphasis added).

#### ISSUE

The issue before us, then, is whether Appellants have shown that the Examiner erred in finding that Sadjadpour anticipates the disputed limitations of independent claims 1, 18, and 23, namely (1) determining a power allocation for at least one bit loading sequence based on minimizing an error rate, and (2) selecting a bit loading sequence with a lowest error rate, as claimed. The issue turns on whether the Examiner's reliance on function 62 in Sadjadpour that jointly minimizes BER and maximizes the total data rate provides sufficient basis for the recited power allocation

determination and bit loading sequence selection limitations. For the following reasons, we find that no such error has been shown.

#### FINDINGS OF FACT

- 1. Sadjadpour discloses a system for minimizing near end cross talk (NEXT) at the central office due to coupling between twisted pairs of wires within cable binders (Sadjadpour, ¶ 0002, 0013-14; Abstract). To this end, a particular function to be optimized is selected from a variety of such functions. *See*, *e.g.*, Functions 61-68 in Figure 6. Based on this selection, a particular bit and power allocation algorithm is implemented responsive to the selection (Sadjadpour, Abstract; ¶ 0043).
- 2. This process is detailed in the flowchart of Figure 6. As shown in that figure, one function that can be selected—Function 62—jointly minimizes the BER and maximizes the total data rate (Sadjadpour, ¶¶ 0044, Fig. 6). Upon selection, the function is inputted to the bit and power allocation algorithm 73 for implementation subject to various constraints and parameters supplied via Blocks 71 and 72 (Sadjadpour, ¶¶ 0045-48).
- 3. Appellants' Specification notes that typical Multiple-Input, Multiple-Output (MIMO) systems comprise a transmitter 2 and receiver 6 with respective multiple antennas that transfer data over a radio channel 4 (Spec. ¶ 0006; Fig. 1). In the transmitter, the modulated signals are sent to a weighting unit that determines weighting factors to allocate power to be transmitted by each antenna (Spec. ¶ 0008). The system, however, can comprise multiple channels, and the channel 4 can be decoupled into a multiple parallel independent sub-channels (eigenmodes) (Spec. ¶ 0010-12).

4. Appellants' Specification notes that various techniques have been used in MIMO systems to apply power to certain channels. One technique known as water-filling maximizes system capacity by determining the optimal power applied as a weighting factor to each of the eigenmodes (Spec. ¶ 0015). This technique not only applies a stronger power weighting factor to better channels, but also implicitly utilizes bit loading by allocating more bits to stronger channels (Spec. ¶ 0016).

## PRINCIPLES OF LAW

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Appl. Dig. Data Sys., Inc.*, 730 F.2d 1440, 1444 (Fed. Cir. 1984); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554 (Fed. Cir. 1983).

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

Discussing the question of obviousness of a patent that claims a combination of known elements, *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007), explains:

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103

likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Sakraida [v. AG Pro, Inc., 425 U.S. 273 (1976)] and Anderson's-Black Rock[, Inc. v. Pavement Salvage Co., 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.* at 1740-41. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 1741 (quoting *In re Kalm*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

#### ANALYSIS

Based on the functionality of Sadjadpour noted in Paragraphs 1 and 2 of the Findings of Fact section *supra*, we find no error in the Examiner's reliance on function 62 in Figure 6 that jointly minimizes BER and maximizes the total data rate. Appellants' argument (Reply Br. 3) that such functionality does not absolutely minimize the BER since it must also maximize the total data rate is unavailing and, in any event, is not commensurate with the scope of the claim language.

Nothing in the language of claims 1, 18, and 23 precludes a power allocation determination based on minimizing an error rate with respect to a particular (e.g., maximized) total data rate. Function 62 of Sadjadpour minimizes the BER for a particular total data rate—a data rate that is maximized. The process of Figure 6 therefore effectively selects a bit loading sequence with a lowest error rate *for that particular data rate* as well as allocating power based on such a selection. Sadjadpour therefore fully meets the disputed limitations of claims 1, 18, and 23.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's anticipation rejection of claims 1, 18, and 23. Therefore, we will sustain the Examiner's rejection of those claims.

The Obviousness Rejection Over Sadjadpour and APA
We now consider the Examiner's obviousness rejection of claims 213, 19, 20, and 22 over Sadjadpour and APA (Ans. 4-6).

#### Claims 2-13

Although Appellants nominally argue the rejection of claims 2-13 separately, Appellants do not particularly point out errors in the Examiner's rejection with respect to the particular limitations of these claims apart from noting that they "recite[] additional limitations" (App. Br. 16-19; Reply Br. 4). Furthermore, Appellants essentially reiterate the same arguments we considered above with respect to claim 1.

Therefore, we will sustain the rejection of these claims for the same reasons discussed above with respect to claim 1. Also, we find that the Examiner has established a prima facie case of obviousness for claims 2-13 that Appellants have not persuasively rebutted. *See Oetiker*, 977 F.2d at 1445.

#### Claim 19

Regarding claim 19, Appellants argue that neither Sadjadpour nor APA teaches or suggests third circuitry for choosing a bit loading sequence having a minimum error rate, as claimed. According to Appellants, Sadjadpour merely selects a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and cross talk (App. Br. 21-22; Reply Br. 4-5).

Appellants' argument, however, is unavailing and simply not commensurate with the scope of the disputed limitation. As we indicated previously, the process of Figure 6 of Sadjadpour effectively selects a bit loading sequence with a lowest error rate for a particular data rate and allocates power based on such a selection. Based on this functionality, we agree with the Examiner (Ans. 12) that the bit loading and power allocation

algorithm in Sadjadpour would, at least implicitly, comprise circuitry for implementing the disputed function (i.e., choosing a bit loading sequence having a minimum BER). As we indicated previously, the fact that this minimum BER is for a particular maximum total data rate does not affect our conclusion.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of representative claim 19. Therefore, we will sustain the Examiner's rejection of that claim.

#### Claim 20

Regarding claim 20, Appellants argue that neither Sadjadpour nor APA teaches or suggests (1) allocating power weighting to a logical channel for minimizing a BER of a corresponding bit loading sequence, and (2) choosing at least one bit loading sequence based on minimizing an error rate, as claimed (App. Br. 23-24; Reply Br. 5-6).

The Examiner indicates that (1) the sub-bands of QAM channels in Sadjadpour or the independent sub-channels in APA correspond to the claimed "logical channels"; (2) the "weighted combination" in Sadjadpour or the "weighting unit" in APA corresponds to the recited "power weighting" limitation; and (3) the BER minimization criteria of the selected function in Figure 6 of Sadjadpour corresponds to minimizing a BER of a corresponding bit loading sequence and the recited bit loading sequence choosing step (Ans. 12-13).

The issue before us, then, is whether Appellants have shown that the Examiner erred in concluding that the disputed limitations of claim 20 would have been obvious to ordinarily skilled artisans based on these collective Application 10/632,089

teachings. For the following reasons, we find that no such error has been shown.

At the outset, we note that our previous discussion regarding Sadjadpour applies equally here and we therefore incorporate that discussion here by reference. Furthermore, Appellants' Specification notes that typical Multiple-Input, Multiple-Output (MIMO) systems comprise a transmitter 2 and receiver 6 with respective multiple antennas that transfer data over a radio channel 4 (Spec. ¶ 0006; Fig. 1). In the transmitter, the modulated signals are sent to a weighting unit that determines weighting factors to allocate power to be transmitted by each antenna (Spec. ¶ 0008). The system, however, can comprise multiple channels, and the channel 4 can be decoupled into a multiple parallel independent sub-channels (eigenmodes) (Spec. ¶ 0010-12).

The Specification notes that various techniques have been used in MIMO systems to apply power to certain channels. One technique known as water-filling maximizes system capacity by determining the optimal power applied as a weighting factor to each of the eigenmodes (Spec. ¶ 0015). This technique not only applies a stronger power weighting factor to better channels, but also implicitly utilizes bit loading by allocating more bits to stronger channels (Spec. ¶ 0016).

Although Sadjadpour pertains to minimizing cross talk over twisted pairs of wires, we find no error in the Examiner's position in applying the fundamental principles of Sadjadpour to MIMO systems. First, we see no reason why ordinarily skilled artisans could not apply the bit and power allocation algorithm implementation of Sadjadpour that minimizes BER for a maximized data rate in an MIMO system, particularly since both systems

pertain to data transmission systems with commensurate modulation schemes. *See*, *e.g.*, Sadjadpour, ¶ 0027 (describing a QAM modulation technique); *see also* Spec. ¶ 0007 (noting that QAM modulation can be employed in MIMO systems).

Second, since both systems employ both power allocation and bit loading techniques, we likewise see no reason why ordinarily skilled artisans could not apply Sadjadpour's bit and power allocation algorithm determination technique to MIMO systems. We recognize that Sadjadpour pertains to reducing cross talk in wired systems using modems, whereas the MIMO systems described in the Specification pertain to communicating data via wireless systems. Nevertheless, these differences do not change our conclusion: they are both in the same field of endeavor (data communications systems) and we find their respective teachings reasonably combinable.

Therefore, since we find that the disputed limitations of claim 20 are reasonably suggested by the collective teachings of the cited prior art, Appellants have not persuaded us of error in the Examiner's rejection of claim 20. We will therefore sustain the Examiner's rejection of claim 20.

#### Claim 22

Regarding claim 22, Appellants essentially reiterate the previouslynoted deficiencies regarding Sadjadpour and APA (App. Br. 7-8; Reply Br. 24-25). Appellants add that the references are not properly combined since ordinarily skilled artisans would allegedly not have considered modifying a twisted pair modem communication technique for application in a wireless communication system (App. Br. 26; Reply Br. 8-9). We find these arguments unavailing, however, for the reasons indicated previously. As such, Appellants have not persuasively rebutted the Examiner's prima facie case of obviousness of claim 22. Since Appellants have not persuaded us of error in the Examiner's rejection of claim 22, the rejection of that claim is therefore sustained.

The Obviousness Rejection Over Sadjadpour, APA, and Kim

We now consider the Examiner's obviousness rejection of claims 1417 and 21 over Sadjadpour, APA, and Kim (Ans. 6-7). Although Appellants nominally argue the rejection of each of these claims separately, Appellants essentially reiterate that the prior art fails to teach or suggest the limitations of claim 1, and add that Kim fails to teach or suggest selecting a bit loading sequence with a lowest error rate as claimed (App. Br. 28-30; Reply Br. 9).

Regarding claim 21, Appellants add that the prior art fails to teach or suggest allocating power weighting to a logical channel for minimizing a BER (App. Br. 30).

We are not persuaded by these arguments for the reasons indicated previously. Nor are these arguments germane to the reason why the Examiner cited the Kim reference and combined its teachings with Sadjadpour and APA (Ans. 6, 15, 16)—a position that we find reasonable. Moreover, Appellants' arguments do not particularly point out errors in the Examiner's rejection with respect to the particular additional limitations of claims 14-17 and 21 apart from noting that they "recite[] additional limitations" (App. Br. 28-30; Reply Br. 9). As such, we find these arguments fall well short of persuasively rebutting the Examiner's prima facie case of obviousness. *See Oetiker*, 977 F.2d at 1445.

Therefore, since Appellants have not persuaded us of error in the Examiner's rejection of claims 14-17 and 21, we will sustain the rejection of these claims

## CONCLUSIONS OF LAW

Appellants have not shown that the Examiner erred in finding that Sadjadpour anticipates the disputed limitations of independent claims 1, 18, and 23 under § 102. Nor have Appellants shown that the Examiner erred in concluding that claims 2-17 and 19-22 would have been obvious to ordinarily skilled artisans at the time of the invention under § 103.

## DECISION

We have sustained the Examiner's rejections with respect to all claims on appeal. Therefore, the Examiner's decision rejecting claims 1-23 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

# **AFFIRMED**

eld

SQUIRE, SANDERS & DEMPSEY L.L.P. 8000 TOWERS CRESCENT DRIVE 14TH FLOOR VIENNA VA 22182-6212